SANT GADGE BABA AMRAVATI UNIVERSITY GAZETTE

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PART- TWO

(Extra-Ordinary)

Friday, the 26th July, 2019

NOTIFICATION

No. 78 /2019 Date : 26 /07/2019

Subject :- Continuation of Prospectus No. 181741 prescribed for Sem. III & IV B.E. (Electronics & Telecommunications) (CGS) for the session 2019-2020 & onwards.

It is notified for general information of all concerned that the Prospectus No.181741 prescribed for Semester **III & IV B.E. (Electronics & Telecommunication Engg.) (CGS)** for the session 2017-2018 and continued upto the session 2018-2019 shall be continued for the academic session 2019-2020 & onwards with substitution of the following subjects as per **Appendix - A** given below :

The remaining subjects in the syllabi of B.E. Sem. III & IV **(**Electronics & Telecommunication Engg**.)** shall remain unchanged.

Sd/-
(Dr.H.R. Deshmukh)
I/c. Registrar
Sant Gadge Baba Amravati University

Appendix – A

SEMESTER - IV

4ET2 – NETWORK ANALYSIS

Course Requisite:

1. (1B4) Electrical Engineering
2. (3ET1) Engineering Mathematics - III

Course Objectives:

1. To understand fundamental concepts of node and mesh analysis for linear circuits.
2. To study graph theory for network analysis.
3. To understand Laplace Transform technique for analysis of linear circuits.
4. To study network theorems and network functions.
5. To study two port network parameters and their inter-relationships.

Course Outcomes:

After successfully completing the course, the students will be able to :

1. Analyze electrical circuits using mesh and node analysis.
2. Draw oriented graph of the network to determine their currents and voltages.
3. Apply Laplace Transform for circuit analysis.
4. Apply suitable network theorems to analyze electrical circuits.
5. Relate various two port network and apply two-port network theory for network analysis.

	Theory : Network Analysis	**L**
Unit-I	**Node and Mesh analysis**: Circuit components, assumptions for circuit analysis; Sources of electrical energy, standard input signals; Source transformation, Kirchoff's laws, Node and Mesh analysis, Network equations for RLC networks, Magnetic coupling.	10
Unit-II	**Graph theory and network equations**: Graph of a network, Trees, cotrees and loops, Incidence matrix, Tie set and Cut set of a network, Analysis of a network using Tie set and Cut set matrix, Network equilibrium equations, Duality.	7
Unit III	**Network Analysis using Laplace Transform**: Review of Laplace transform, Gate function, Impulse function, Laplace transform of periodic signals, Transformed equivalent of inductance, capacitance, mutual inductance, Node and mesh analysis of the transformed circuits. Node admittance matrix and Mesh impedance matrix in transform domain.	8
Unit-IV	**Network theorems**: Superposition theorem, Receprocity theorem, Thevenin's theorem, Norton's theorem, Millman's theorem, Maximum power transfer theorem.	10
Unit-V	**Network functions**: Ports and terminal pairs, Network functions, poles and zeros, Necessary conditions for driving point function, Necessary conditions for transfer function, Application of network analysis in deriving functions, Time domain behaviour from pole-zero plot, driving point and transfer impedance functions of LC networks.	6

Unit-VI	**Two port networks**: Open circuit impedance parameters, Short circuit admittance parameters, Transmission parameters, Hybrid parameters, Condition for reciprocity and symmetry of a two port network, Interrelationship between parameters, Interconnection of two port networks, Input impedance in terms of two port network parameters, Output impedance, Image impedance.	9
	Total	**52**

Text Book: D. Roy Choudhary, "Networks and Systems", New Age International.

References:

1. M. E. Van Valkenburg, "Network Analysis", Prentice Hall, 3rd Edition.
2. W. H. Hayt, J. E. Kemmerly & S. M. Durbin, "Engineering Circuit Analysis", 7th Edn, McGraw-Hill higher education.
3. C. K. Alexander and M. N. O. Sadiku, "Fundamentals of Electric Circuit" McGraw-Hill Companies.inc.
4. I.S.K.V. Iyer, "Circuit Theory", Tata McGraw-Hill Education 1985.

4ET4 – DIGITAL ELECTRONICS

Course Requisite:

1. (3ET3) Electronic Devices & Circuits

Course Objectives:

1. To study basic concepts of Boolean algebra, number systems and codes.
2. To study techniques of minimization of Boolean expression.
3. To learn digital logic families and their characteristics.
4. To study the formal procedures for the analysis and design of combinational circuits and sequential circuits.
5. To learn the concept of memories, programmable logic devices and digital ICs.

Course Outcomes:

After successfully completing the course, the students will be able to

1. Use Boolean algebra to solve logic functions, number systems and its conversion.
2. Understand digital logic families and their characteristics.
3. Identify, analyze and design combinational and sequential circuits.
4. Use the knowledge of semiconductor memories, programmable logic devices in digital design.

	Theory :Digital Electronics	**L**
Unit-I	Boolean Algebra, Number systems and their conversions, BCD code, Octal Code, Hexadecimal code, Excess-3 code, Gray code, Arithmetic operations using Two's compliment. Study and analysis of Digital Logic Families : RTL, TTL, ECL, IIL, CMOS and their characteristics, tri-state logic, Logic gates	10
Unit-II	Combinational Logic Design: Functions of binary variables, Standard form of logic functions, K-Map up to 5 variables, Don't Care Condition and its effect, Simplification of logic expressions using K-Map, adders and subtractors using logic gates, 4 bit adder/subtractor, BCD adder/subtractor, Look ahead carry adder.	08
Unit-III	Combinational logic design using 74XX/54XX MSI chip series concerning to MUX, DEMUX, Decoders, Encoders, Code Converters, Comparators, Parity Generator/Checker and BCD to Seven Segment Decoder. Combinational logic design using ROM, PLA, PAL.	08
Unit-IV	Flip-flops: R-S, J-K, Master slave J-K, D-type, T-type. Registers: SISO, SIPO, PISO, PIPO, Universal Shift Register. Counters: Asynchronous and Synchronous counter, up/down counter, MOD-N counter, Ring counter, Johnson counter, Frequency Division counter.	10
Unit-V	Analysis of Clocked Sequential Networks, Moore and Mealy Machine, State table, State Reduction State Transition diagram, Design of clocked sequential networks.	08
Unit-VI	Semiconductor memories and Programmable Logic Devices: memory organization and operation, expanding memory size, Classification and characteristics of memories, RAM, ROM, EPROM, EEPROM, NVRAM, SRAM, DRAM. Introduction to FPGA & CPLD.	08
	Total	**52**

Text Books:

1. M.Morris Mano and M.D.Ciletti, "Digital Design", Pearson Education.
2. R P Jain, "Modern Digital Electronics", TMH.

References:

1. Wakerly, "Digital Design: Principles and Practices", 3rd edition, Pearson Education, 2004.
2. Charles H. Roth, "Fundamentals of Logic Design", 4th Edition, Jaico Publication
3. Lee S.C,"Digital Circuits and Logic Design", PHI.

4ETp8 – DIGITAL ELECTRONICS – LAB.

Course Requisite:

1. (3ET3) Electronic Devices & Circuits.
2. (4ET4) Digital Electronics.

Course Objectives:

1. To impart the concepts of digital electronics practically.
2. To provide students basic experimental experiences in the operation of various digital logic Families.
3. To learn the operation of various logic gates and their implementation using digital IC's.
4. To learn the realization of various combinational and sequential circuits.

Course Outcomes:

After successfully completing the course, the students will be able to :

1. Apply practically the concepts of digital electronics.
2. Explain the operation and characteristics of various digital logic families.
3. Understand the operation of various logic gates and their implementation using digital IC's.
4. Design and implement various combinational logic circuits.
5. Design and implement various sequential logic circuits.

Exp.No.	Expeeriment List :
Exp-1	To study and verify the operation of various digital logic families.
Exp -2	To study and verify the operation of logic gates.
Exp -3	Design and implementation of Adders and Subtractors using logic gates.
Exp -4	Design and implementation of code converters using logic gates.
Exp -5	Design and implementation of multiplexer using logic gates and IC.
Exp -6	Design and implementation of demultiplexer using logic gates and IC.
Exp -7	Design and implementation of code converters using logic gates.
Exp -8	Design and implementation of Magnitude Comparator using logic gates and IC.
Exp -9	Design and implementation of odd/even parity checker /generator using IC.
Exp -10	Implementation of SISO, SIPO, PISO and PIPO shift registers using Flip- flops.
Exp -11	Construction and verification of ripple counters.
Exp -12	Design and implementation of 3-bit synchronous up/down counter.

* Minimum 10 experiments based on/relevant to the above list.

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NOTIFICATION

No. 79 /2019 Date : 26/07/2019

Subject :- Continuation of Prospectus No. 181712 prescribed for Sem. V & VI B.E. (Electronnics & Telecommunications) (CGS) for the session 2019-2020& onwards.

It is notified for general information of all concerned that the Prospectus No. 181712 prescribed for Semester **V & VI B.E. (Electronics & Telecommunication Engg.) (CGS)** for the session 2018-2019 shall be continued for the academic session 2019-2020 & onwards with substitution of the following subjects as per **Appendix –A** given below :

The remaining subjects in the syllabi of B.E. Sem. V & VI **(**Electronics & Telecommunication Engg**.)** shall remain unchanged.

Sd/-
(Dr.H.R. Deshmukh)
I/c. Registrar
Sant Gadge Baba Amravati University